

## -40V P-Channel Enhancement Mode MOSFET

### Description

The AP6P04SI uses advanced trench technology to provide excellent  $R_{DS(ON)}$ , low gate charge and operation with gate voltages as low as 4.5V. This device is suitable for use as a Battery protection or in other Switching application.

### General Features

$V_{DS} = -40V$   $I_D = -6.8A$

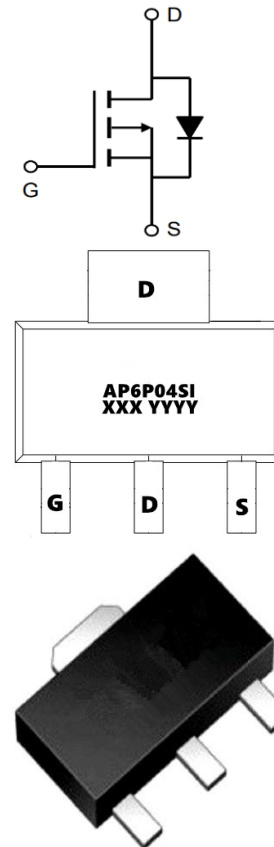
$R_{DS(ON)} < 72m\Omega$  @  $V_{GS} = -10V$  (Type: 65m $\Omega$ )

### Application

Battery protection

Load switch

Uninterruptible power supply



### Package Marking and Ordering Information

Product ID	Pack	Marking	Qty(PCS)
AP6P04SI	SOT89-3L	AP6P04SI XXX YYYY	3000

### Absolute Maximum Ratings ( $T_C = 25^\circ C$ unless otherwise noted)

Symbol	Parameter	Steady State	Units
$V_{DS}$	Drain-Source Voltage	-40	V
$V_{GS}$	Gate-Source Voltage	$\pm 20$	V
$I_D @ T_A = 25^\circ C$	Continuous Drain Current, $V_{GS} @ -4.5V^1$	-6.8	A
$I_D @ T_A = 70^\circ C$	Continuous Drain Current, $V_{GS} @ -4.5V^1$	-3.3	A
IDM	Pulsed Drain Current <sup>2</sup>	-16.1	A
$P_D @ T_A = 25^\circ C$	Total Power Dissipation <sup>3</sup>	1.32	W
$P_D @ T_A = 70^\circ C$	Total Power Dissipation <sup>3</sup>	0.84	W
TSTG	Storage Temperature Range	-55 to 150	$^\circ C$
$T_J$	Operating Junction Temperature Range	-55 to 150	$^\circ C$
$R_{\theta JA}$	Thermal Resistance Junction-Ambient <sup>1</sup>	85	$^\circ C/W$
$R_{\theta JC}$	Thermal Resistance Junction-Case <sup>1</sup>	80	$^\circ C/W$

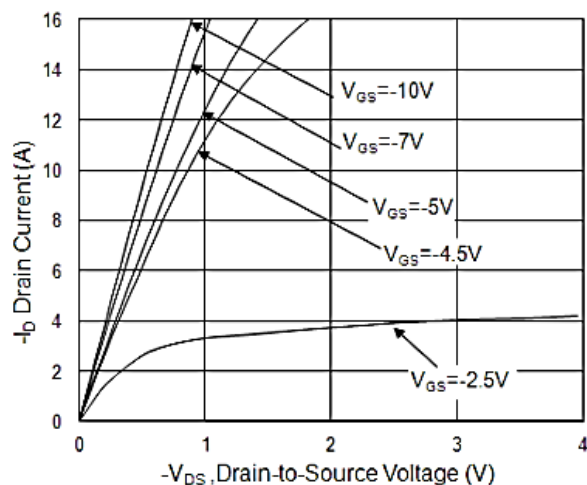
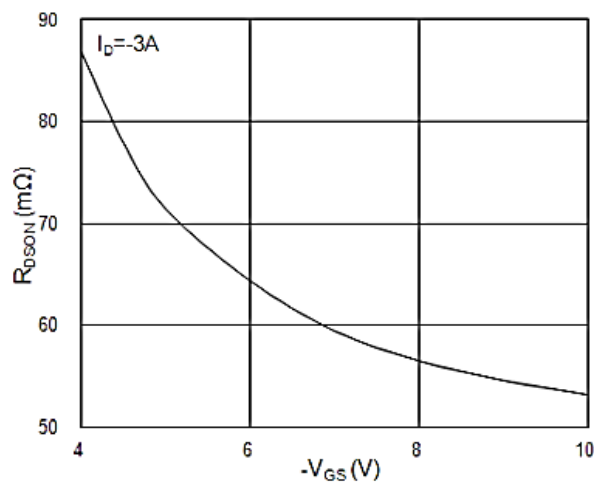
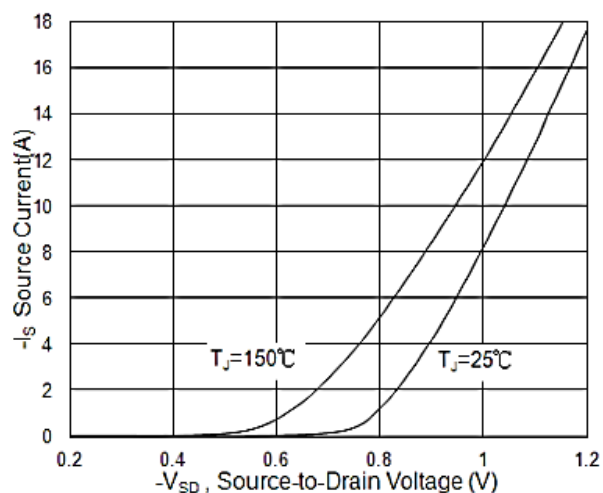
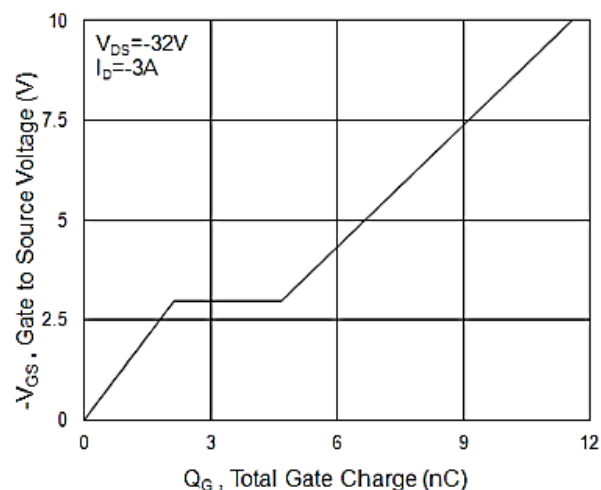
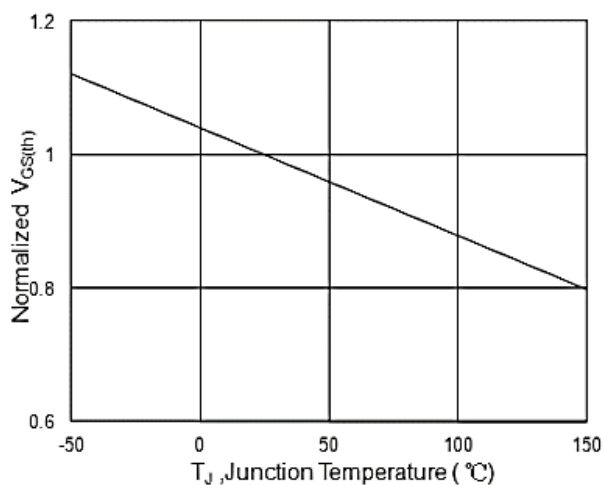
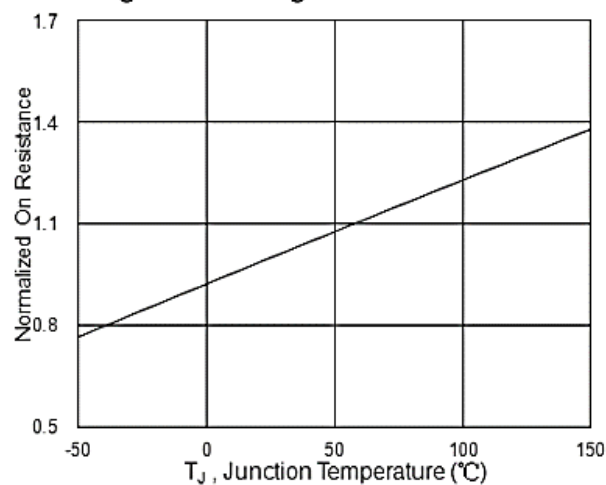
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### Electrical Characteristics (T<sub>J</sub>=25°C, unless otherwise noted)

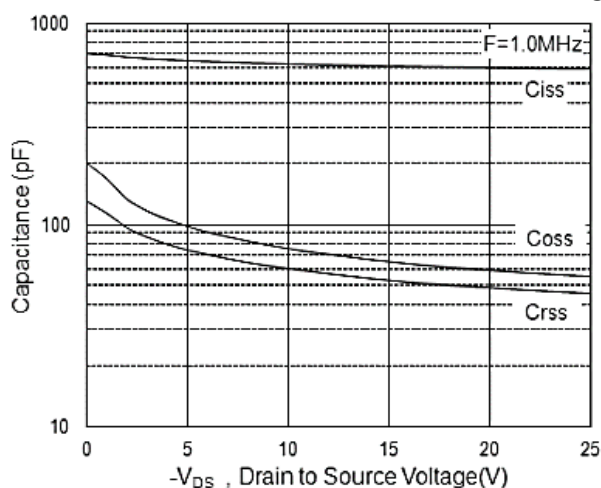
Symbol	Parameter	Conditions	Min.	Typ	Max.	Unit
BVDSS	Drain-Source Breakdown Voltage	V <sub>GS</sub> =0V, I <sub>D</sub> =-250uA	-40	-46	---	V
ΔBVDSS/ΔT <sub>J</sub>	BV <sub>DSS</sub> Temperature Coefficient	Reference to 25°C, I <sub>D</sub> =-1mA	---	-0.018	---	V/°C
RDS(ON)	Static Drain-Source On-Resistance <sup>2</sup>	V <sub>GS</sub> =-4.5V, I <sub>D</sub> =-3A	---	65	72	mΩ
		V <sub>GS</sub> =-2.5V, I <sub>D</sub> =-2A	---	89	100	
VGS(th)	Gate Threshold Voltage	V <sub>GS</sub> =V <sub>DS</sub> , I <sub>D</sub> =-250uA	-1.0	-1.5	-2.5	V
ΔVGS(th)	VGS(th) Temperature Coefficient		---	2.5	---	mV/°C
IDSS	Drain-Source Leakage Current	V <sub>DS</sub> =-24V, V <sub>GS</sub> =0V, T <sub>J</sub> =25°C	---	---	-1	uA
		V <sub>DS</sub> =-24V, V <sub>GS</sub> =0V, T <sub>J</sub> =55°C	---	---	-5	
IGSS	Gate-Source Leakage Current	V <sub>GS</sub> =±20V, V <sub>DS</sub> =0V	---	---	±100	nA
gfs	Forward Transconductance	V <sub>DS</sub> =-5V, I <sub>D</sub> =-3A	---	5.8	---	S
Q <sub>g</sub>	Total Gate Charge (-4.5V)	V <sub>DS</sub> =-32V, V <sub>GS</sub> =-4.5V, I <sub>D</sub> =-3A	---	6.4	---	nC
Qgs	Gate-Source Charge		---	2.1	---	
Qgd	Gate-Drain Charge		---	2.5	---	
Td(on)	Turn-On Delay Time	V <sub>DD</sub> =-20V, V <sub>GS</sub> =-4.5V, R <sub>G</sub> =3.3Ω, I <sub>D</sub> =-3A	---	4.2	---	ns
T <sub>r</sub>	Rise Time		---	23	---	
Td(off)	Turn-Off Delay Time		---	26.8	---	
T <sub>f</sub>	Fall Time		---	20.6	---	
Ciss	Input Capacitance	V <sub>DS</sub> =-15V, V <sub>GS</sub> =0V, f=1MHz	---	620	---	pF
Coss	Output Capacitance		---	65	---	
Crss	Reverse Transfer Capacitance		---	53	---	
IS	Continuous Source Current <sup>1,4</sup>	V <sub>G</sub> =V <sub>D</sub> =0V, Force Current	---	---	-5.2	A
ISM	Pulsed Source Current <sup>2,4</sup>		---	---	-16.1	A
VSD	Diode Forward Voltage <sup>2</sup>	V <sub>GS</sub> =0V, I <sub>S</sub> =-1A, T <sub>J</sub> =25°C	---	---	-1	V

#### Note :

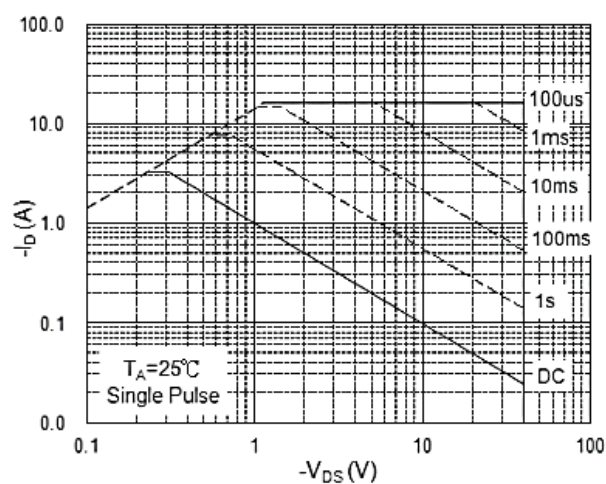
- 1、The data tested by surface mounted on a 1 inch FR-4 board with 2OZ copper.
- 2、The data tested by pulsed , pulse width ≤ 300us , duty cycle ≤ 2%
- 3、The power dissipation is limited by 150°C junction temperature
- 4、The data is theoretically the same as I<sub>D</sub> and I<sub>DM</sub> , in real applications , should be limited by total power dissipation.

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**Typical Characteristics**

**Fig.1 Typical Output Characteristics**

**Fig.2 On-Resistance vs. G-S Voltage**

**Fig.3 Forward Characteristics Of Reverse**

**Fig.4 Gate-Charge Characteristics**

**Fig.5 Normalized  $V_{GS(th)}$  vs.  $T_J$** 

**Fig.6 Normalized  $R_{DS(on)}$  vs.  $T_J$**

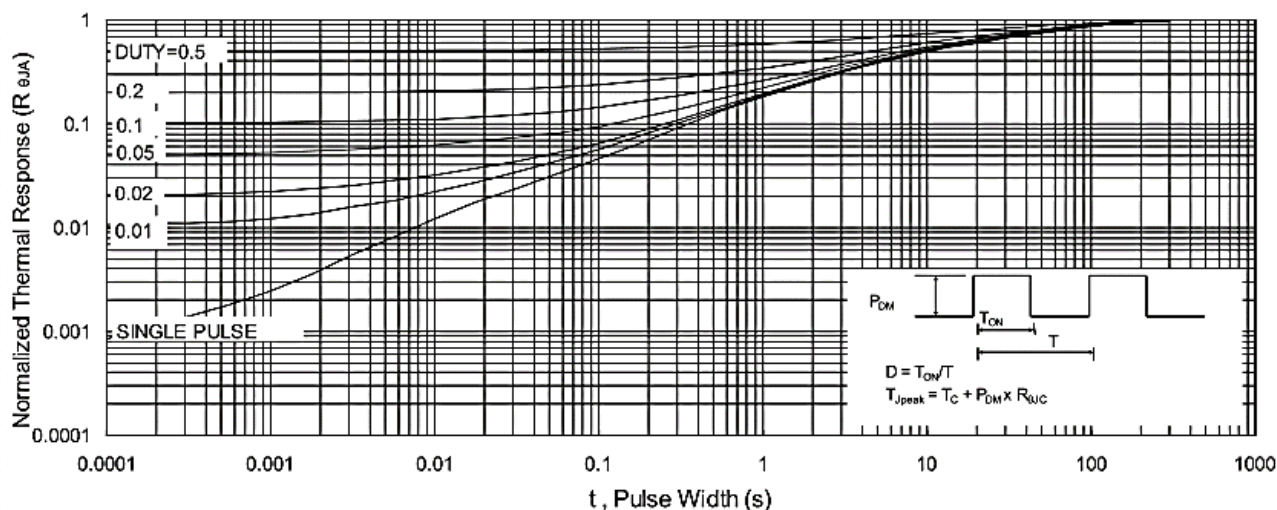
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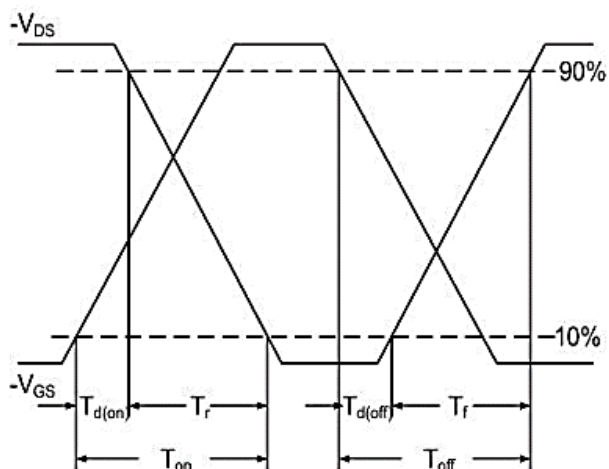
**Fig.7 Capacitance**



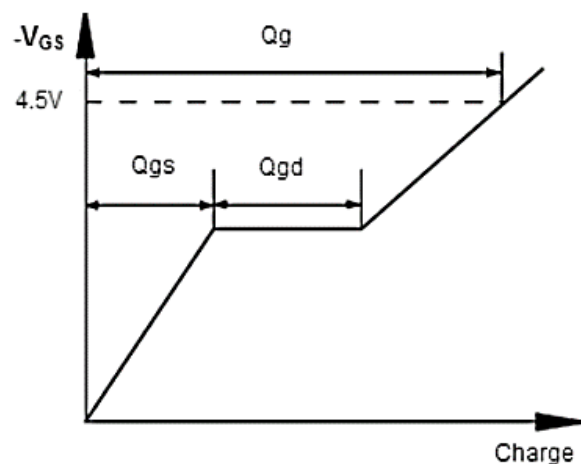
**Fig.8 Safe Operating Area**



**Fig.9 Normalized Maximum Transient Thermal Impedance**



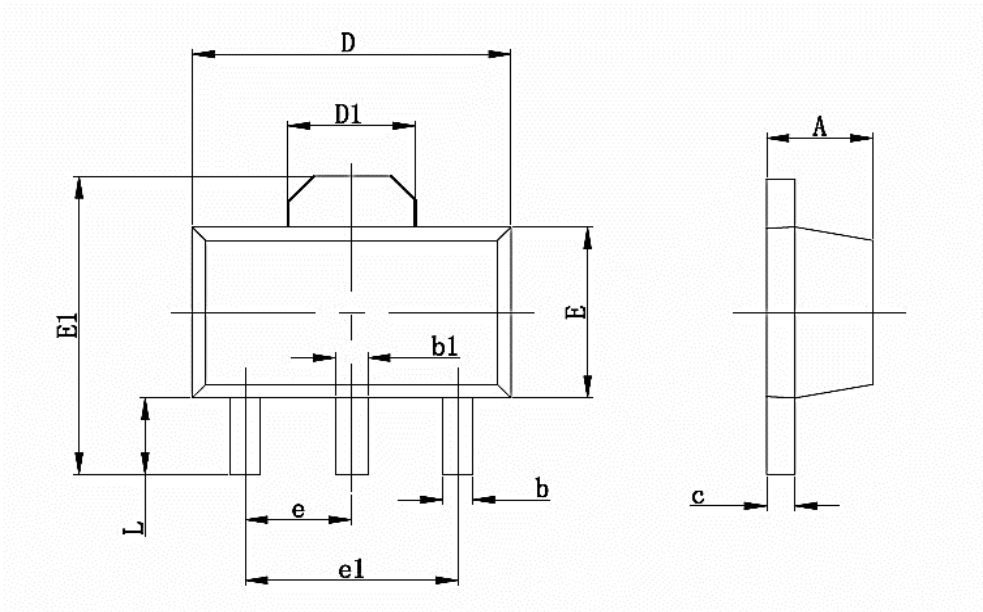
**Fig.10 Switching Time Waveform**



**Fig.11 Gate Charge Waveform**

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Package Mechanical Data:SOT89-3L



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.400	1.600	0.055	0.063
b	0.350	0.520	0.013	0.197
b1	0.400	0.580	0.016	0.023
c	0.350	0.440	0.014	0.017
D	4.400	4.600	0.173	0.181
D1	1.550 REF		0.061 REF	
E	2.350	2.550	0.091	0.102
E1	3.940	4.250	0.155	0.167
e	1.500 TYP		0.060TYP	
e1	3.000 TYP		0.118TYP	
L	0.900	1.100	0.035	0.047