



Description

The FIR150N085ANFG uses advanced trench technology and design to provide excellent $R_{DS(ON)}$ with low gate charge. It can be used in Automotive applications and a wide variety of other applications.

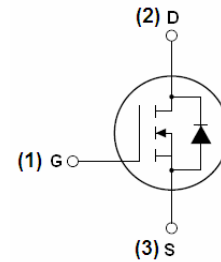
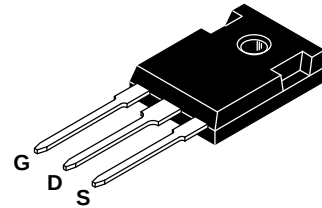
General Features

- $V_{DSS} = 85V, I_D = 210A$
 $R_{DS(ON)} < 4.5m\Omega @ V_{GS} = 10V$
- Good stability and uniformity with high E_{AS}
- Special process technology for high ESD capability
- High density cell design for ultra low $R_{DS(on)}$
- Fully characterized Avalanche voltage and current
- Excellent package for good heat dissipation

Application

- Automotive applications
- Hard Switched and High Frequency Circuits
- Uninterruptible Power Supply

PIN Connection TO-247



Marking Diagram



Y = Year
A = Assembly Location
WW = Work Week
FIR150N085ANF = Specific Device Code

Package Marking And Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
FIR150N085ANF	FIR150N085ANFG	TO-247	-	-	-

Absolute Maximum Ratings (TA=25°C unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DSS}	85	V
Gate-Source Voltage	V_{GS}	± 20	V
Drain Current-Continuous	I_D	210	A
Drain Current-Continuous($T_C = 100^\circ C$)	$I_D (100^\circ C)$	150	A
Pulsed Drain Current	I_{DM}	850	A
Maximum Power Dissipation	P_D	330	W
Derating factor		2.2	W/°C
Single pulse avalanche energy (Note 3)	E_{AS}	2200	mJ
Peak Diode Recovery dv/dt (Note 4)	dv/dt	5	V/ns
Operating Junction and Storage Temperature Range	T_J, T_{STG}	-55 To 175	°C



Thermal Characteristic

Thermal Resistance, Junction-to-Case (Note 1)	$R_{\theta JC}$	0.45	$^{\circ}\text{C/W}$
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Electrical Characteristics (TA=25°C unless otherwise noted)

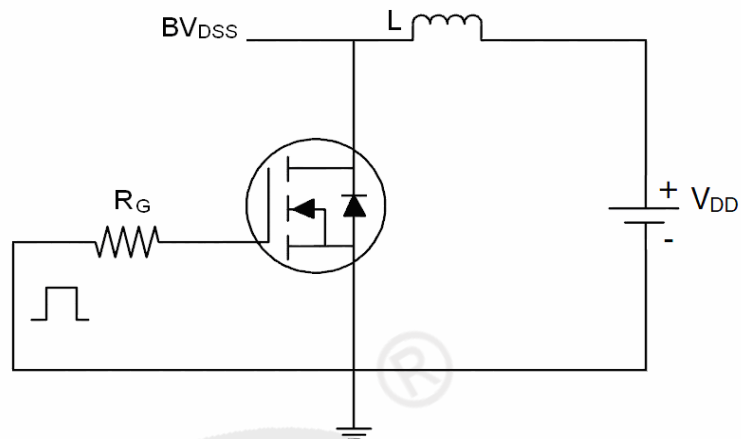
Parameter		Symbol	Condition	Min	Typ	Max	Unit
Off Characteristics							
Drain-Source Breakdown Voltage		BV _{DSS}	V _{GS} =0V I _D =250μA	85	-	-	V
Zero Gate Voltage Drain Current		I _{DSS}	V _{DS} =85V, V _{GS} =0V	-	-	1	μA
Gate-Body Leakage Current		I _{GSS}	V _{GS} =±20V, V _{DS} =0V	-	-	±200	nA
On Characteristics							
Gate Threshold Voltage		V _{GS(th)}	V _{DS} =V _{GS} , I _D =250μA	2	3	4	V
Drain-Source On-State Resistance	25°C	R _{DS(ON)}	V _{GS} =10V, I _D =40A	-	3.2	4.5	mΩ
	125°C			-	5	6.8	mΩ
Forward Transconductance		g _{FS}	V _{DS} =25V, I _D =40A	100	165	-	S
Dynamic Characteristics							
Input Capacitance		C _{iss}	V _{DS} =25V, V _{GS} =0V, F=1.0MHz	-	12100	-	PF
Output Capacitance		C _{oss}		-	2000	-	PF
Reverse Transfer Capacitance		C _{rss}		-	480	-	PF
Switching Characteristics							
Turn-on Delay Time		t _{d(on)}	V _{DD} =38V, I _D =40A V _{GS} =10V, R _{GEN} =1.2Ω (Note2)	-	20	-	nS
Turn-on Rise Time		t _r		-	190	-	nS
Turn-Off Delay Time		t _{d(off)}		-	130	-	nS
Turn-Off Fall Time		t _f		-	120	-	nS
Total Gate Charge		Q _g	V _{DS} =60V, I _D =40A, V _{GS} =10V(Note2)	-	410	620	nC
Gate-Source Charge		Q _{gs}		-	90	140	nC
Gate-Drain Charge		Q _{gd}		-	140	210	nC
Drain-Source Diode Characteristics							
Diode Forward Voltage		V _{SD}	V _{GS} =0V, I _S =40A	-	-	1.2	V
Reverse Recovery Time		t _{rr}	T _J = 25°C, I _F = 40A di/dt = 100A/μs(Note2)	-	120	210	nS
Reverse Recovery Charge		Q _{rr}		-	860	1300	nC
Forward Turn-On Time		t _{on}	Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD)				

Notes:

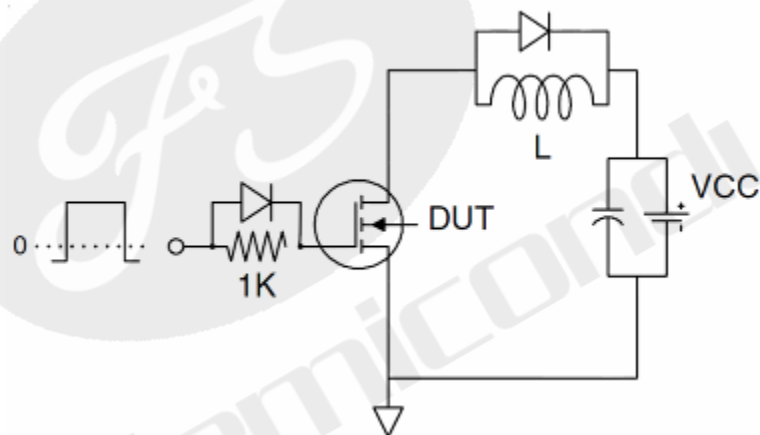
1. Surface Mounted on FR4 Board, $t \leq 10$ sec.
2. Pulse Test: Pulse Width $\leq 400\mu s$, Duty Cycle $\leq 2\%$.
3. EAS condition: $T_J=25^{\circ}\text{C}, V_{DD}=42.5V, V_G=10V, L=2mH, R_g=25\Omega, I_{AS}=37A$
4. $I_{SD} \leq 125A, di/dt \leq 260A/\mu s, V_{DD} \leq V_{(BR)DSS}, T_J \leq 175^{\circ}\text{C}$

Test circuit

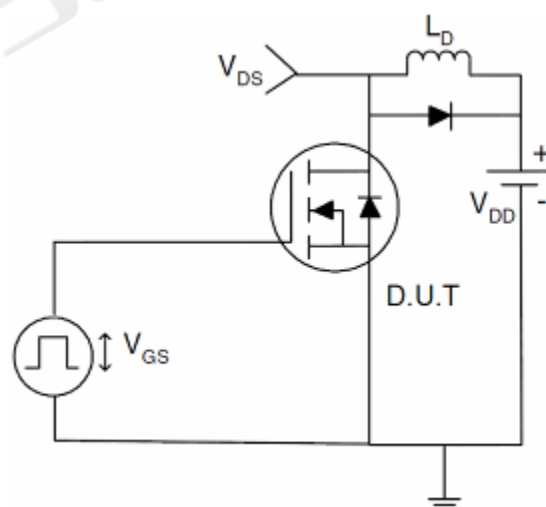
1) E_{AS} test Circuits



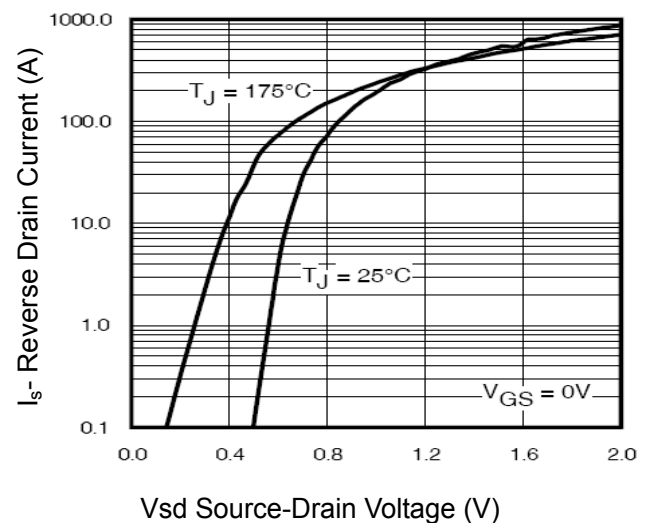
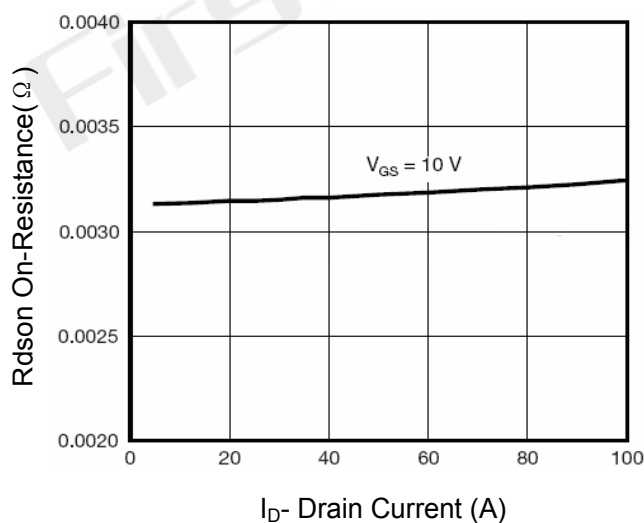
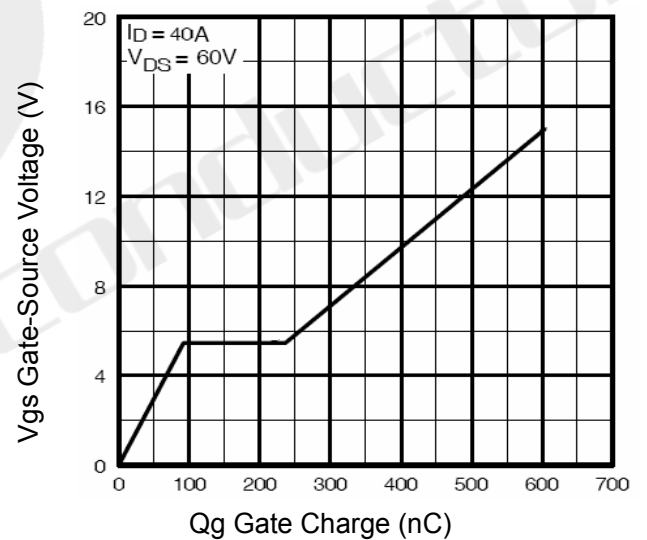
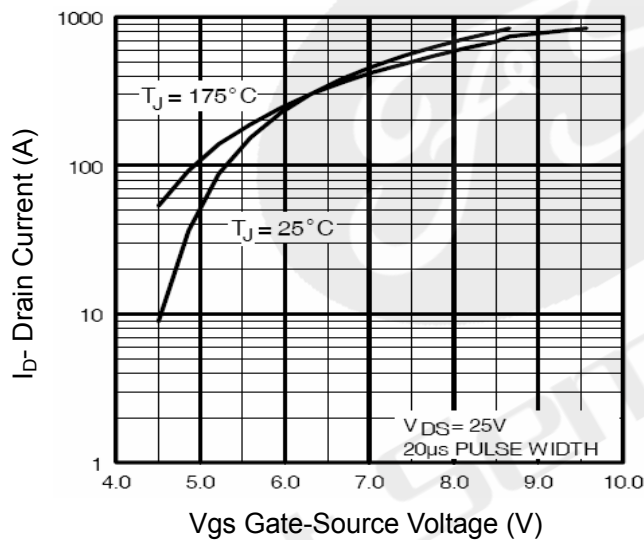
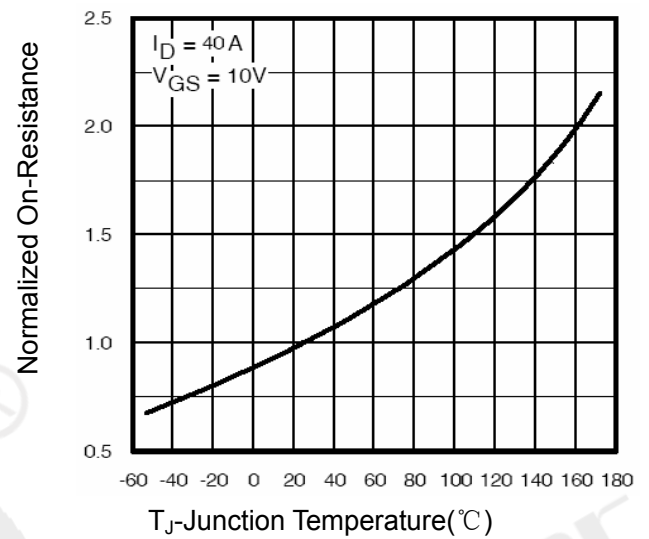
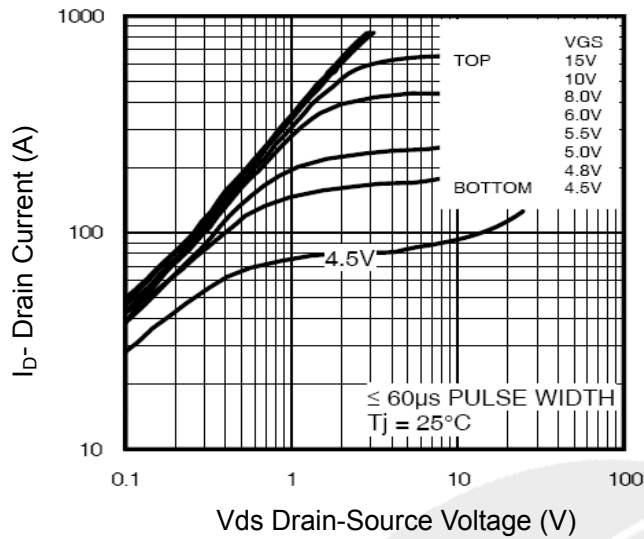
2) Gate charge test Circuit:



3) Switch Time Test Circuit:



Typical Electrical And Thermal Characteristics(Curves)



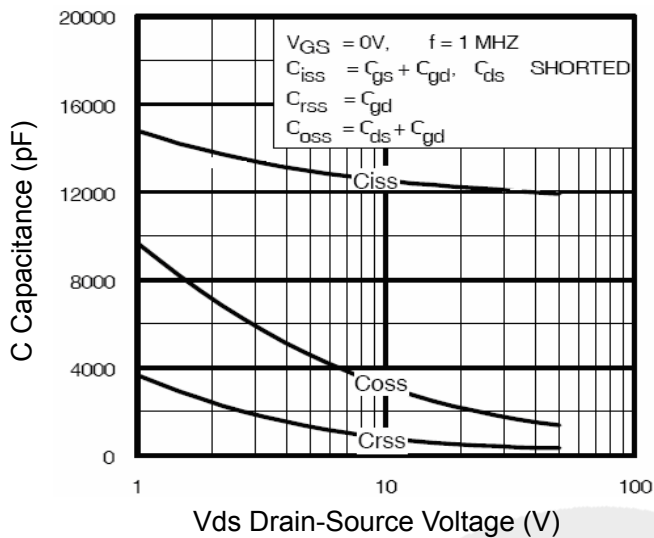


Figure 7 Capacitance vs Vds

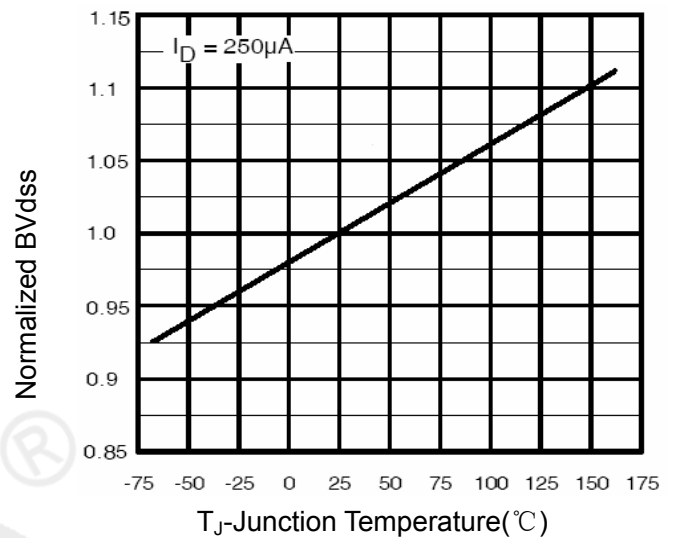
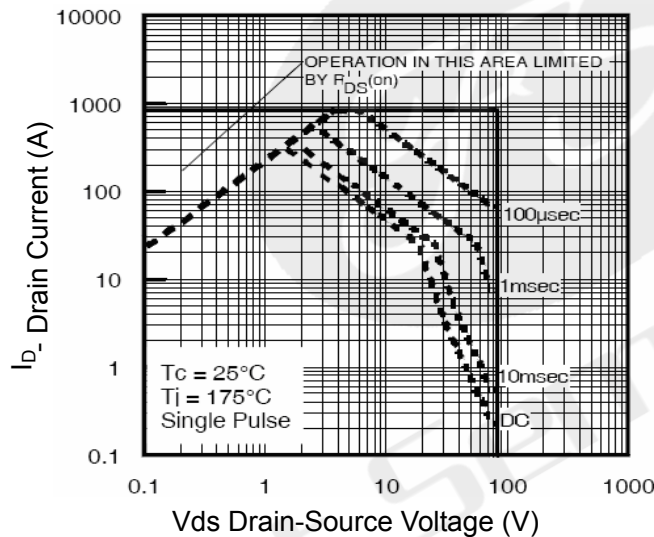

Figure 9 BV_{DSS} vs Junction Temperature


Figure 8 Safe Operation Area

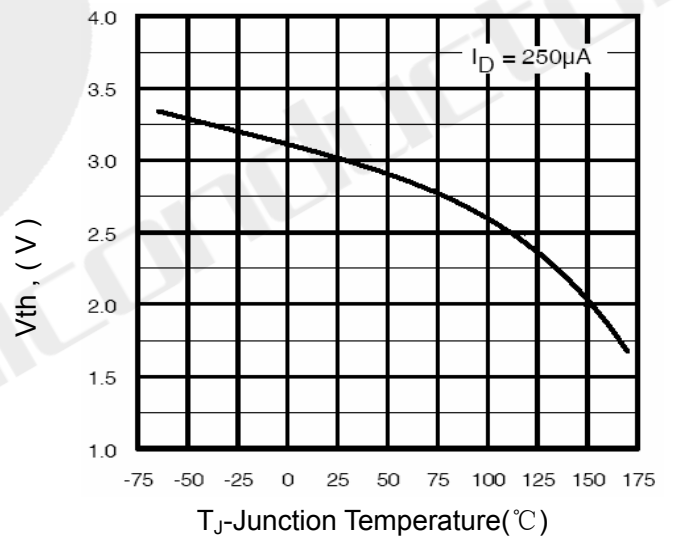
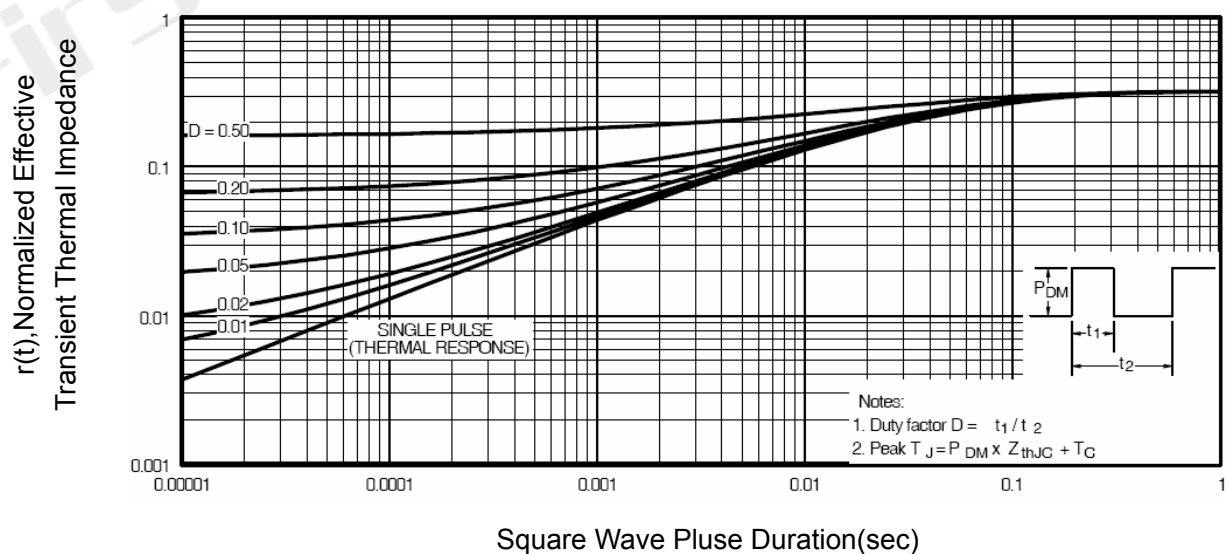
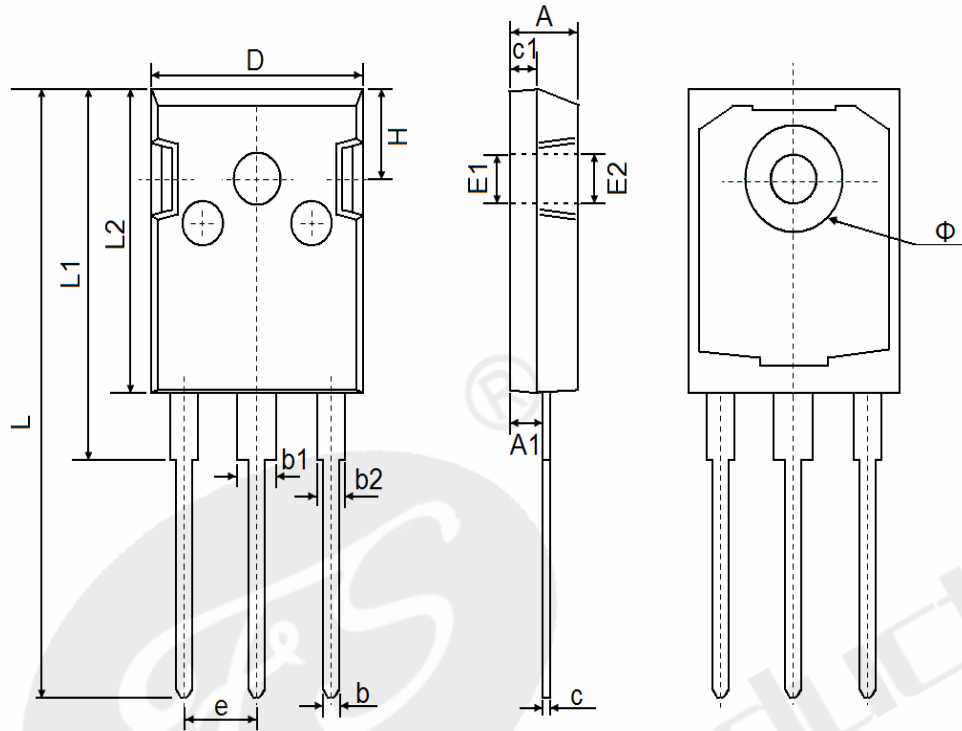

Figure 10 $V_{GS(th)}$ vs Junction Temperature


Figure 11 Normalized Maximum Transient Thermal Impedance

Package Information



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	4.850	5.150	0.191	0.200
A1	2.200	2.600	0.087	0.102
b	1.000	1.400	0.039	0.055
b1	2.800	3.200	0.110	0.126
b2	1.800	2.200	0.071	0.087
c	0.500	0.700	0.020	0.028
c1	1.900	2.100	0.075	0.083
D	15.450	15.750	0.608	0.620
E1	3.500 REF		0.138 REF	
E2	3.600 REF		0.142 REF	
L	40.900	41.300	1.610	1.626
L1	24.800	25.100	0.976	0.988
L2	20.300	20.600	0.799	0.811
Φ	7.100	7.300	0.280	0.287
e	5.450 TYP		0.215 TYP	
H	5.980 REF		0.235 REF	



Declaration

- FIRST reserves the right to change the specifications, the same specifications of products due to different packaging line mold, the size of the appearance will be slightly different, shipped in kind, without notice! Customers should obtain the latest version information before ordering, and verify whether the relevant information is complete and up-to-date.
- Any semiconductor product under certain conditions has the possibility of failure or failure, The buyer has the responsibility to comply with safety standards and take safety measures when using FIRST products for system design and manufacturing, To avoid To avoid potential failure risks, which may cause personal injury or property damage!
- Product promotion endless, our company will wholeheartedly provide customers with better products!

ATTACHMENT

Revision History

Date	REV	Description	Page
2018.01.01	1.0	Initial release	